

FIG. 1

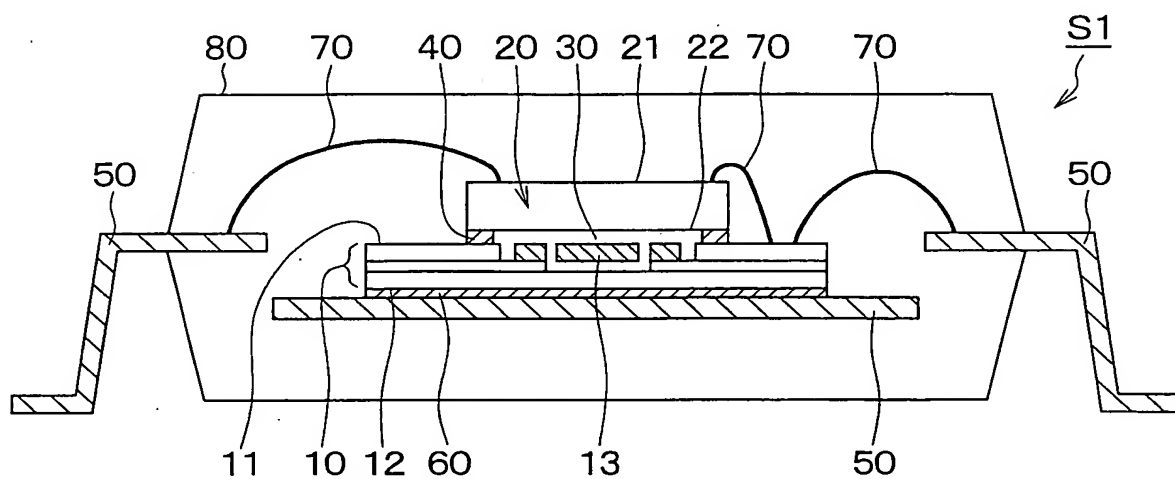
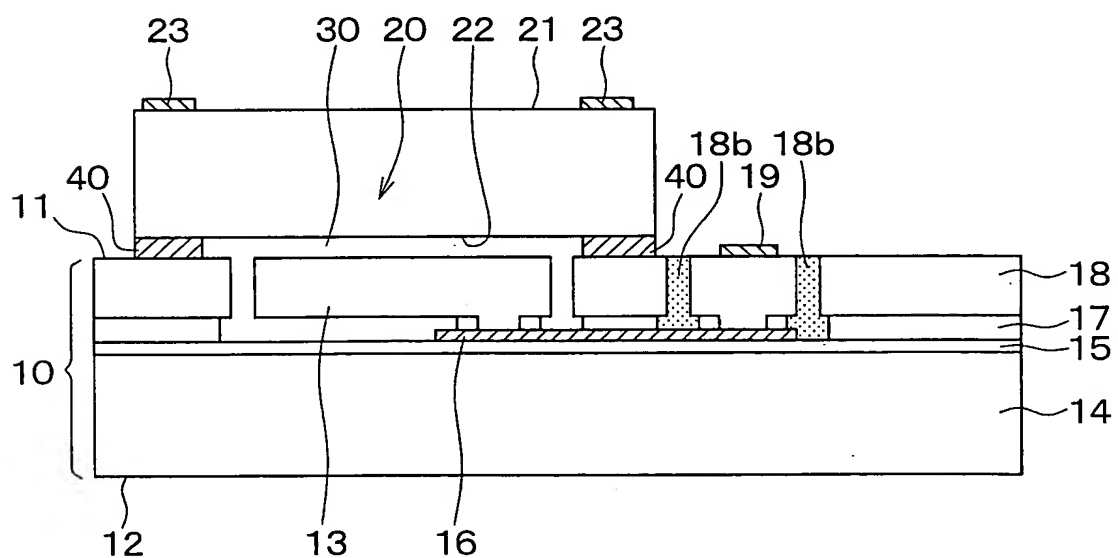


FIG. 3



[illegible]

FIG. 4

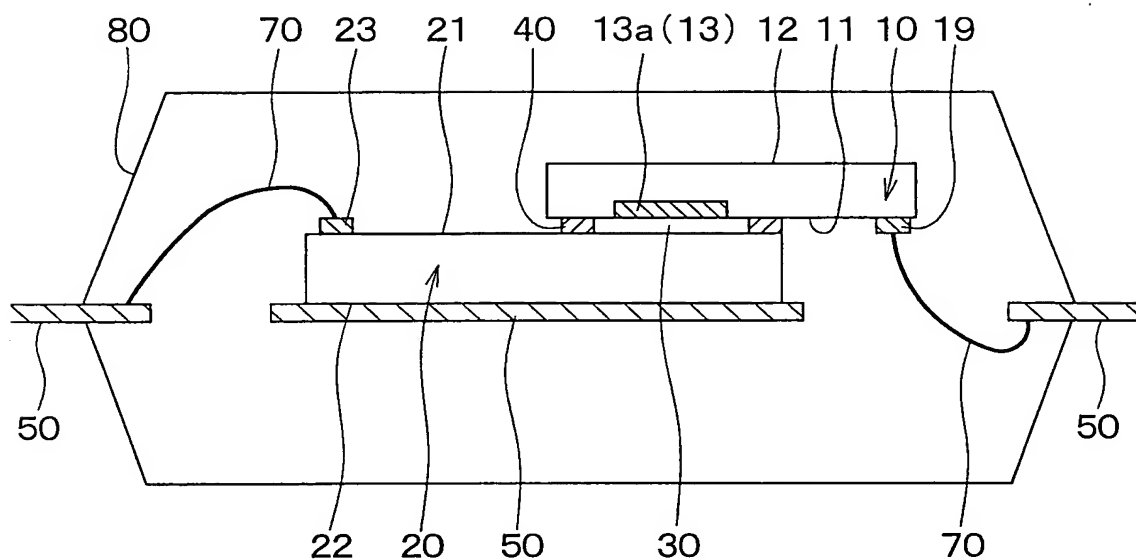


FIG. 5

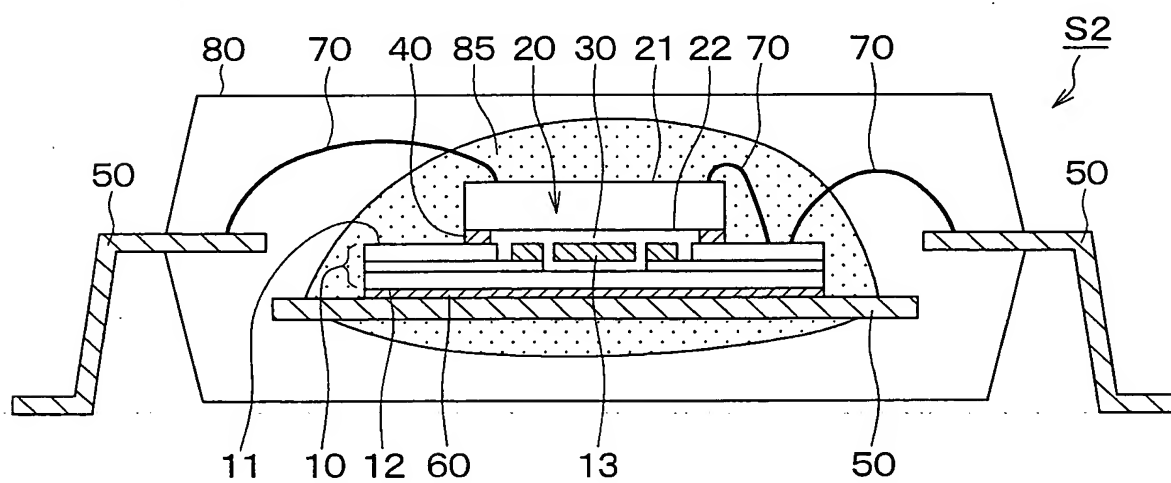


FIG. 6

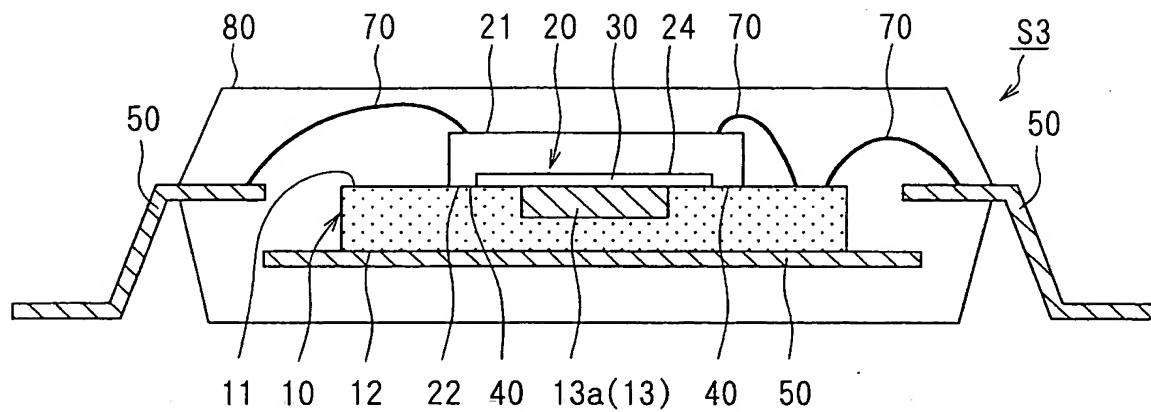


FIG. 7

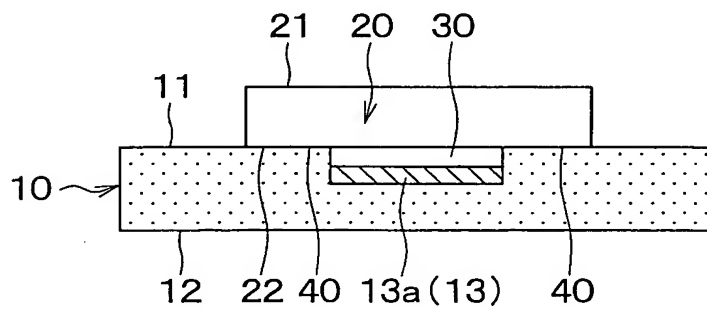


FIG. 8

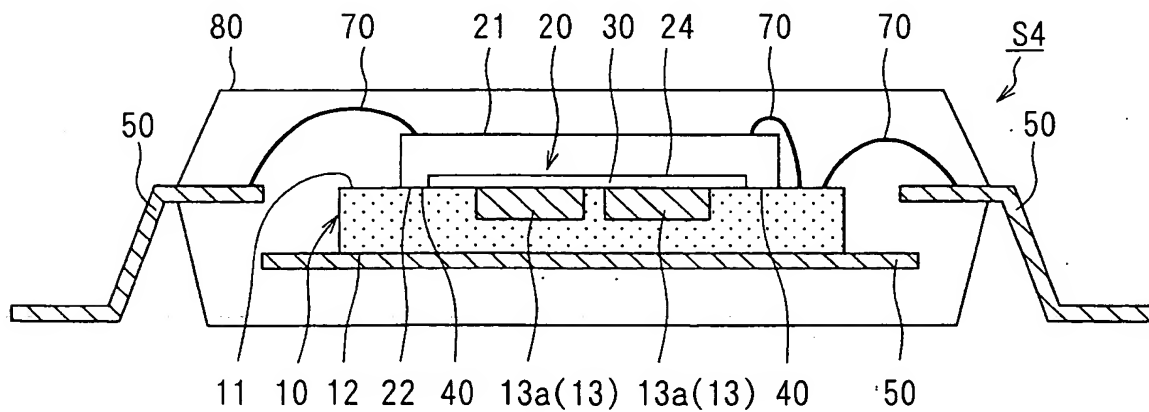


FIG. 9

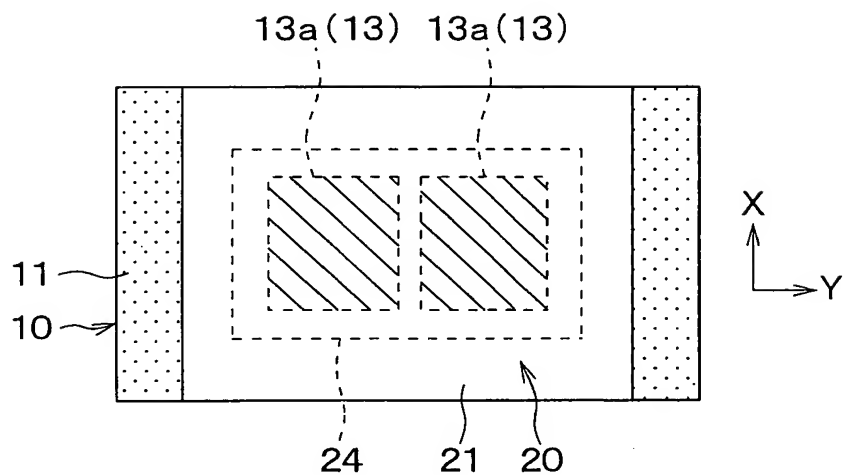
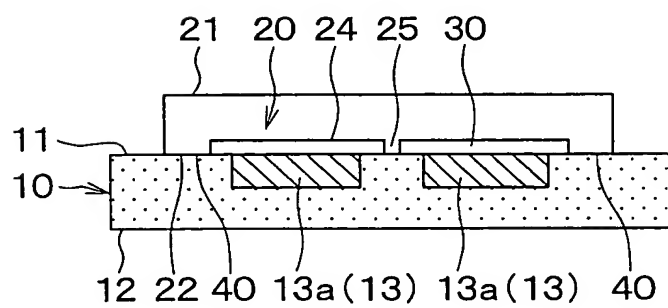
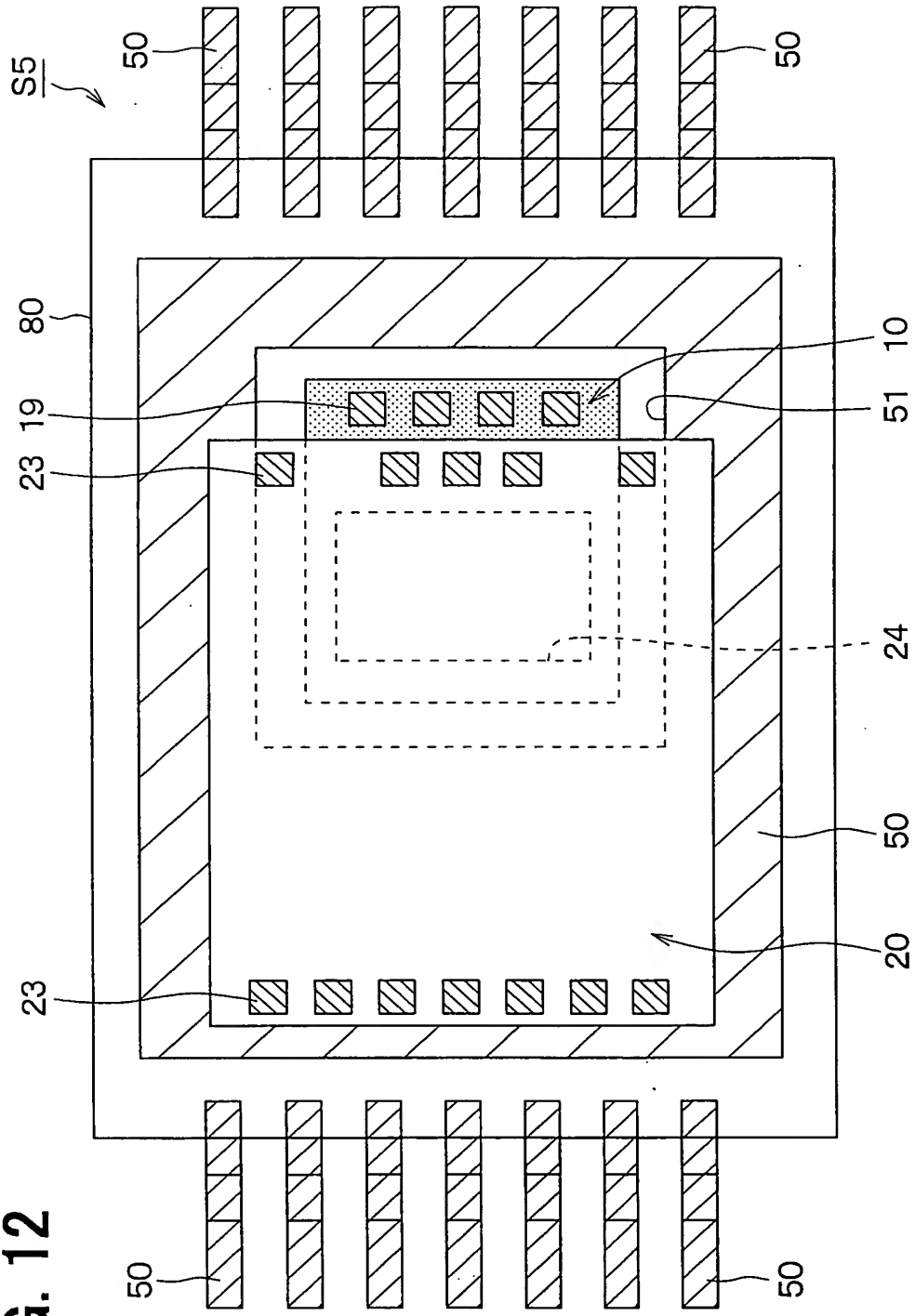


FIG. 10



[illegible]

FIG. 12



[illegible]

A cross-sectional view of a semiconductor device. It features a central channel region (10) with a dotted pattern, flanked by side gate regions (11, 12) with a stippled pattern. A gate stack (20, 20a) is positioned on top of the channel. A source/drain region (30) is located on the right side of the channel. The device is surrounded by a substrate (50) and a top layer (80). Various other regions and layers are labeled with numbers: 70, 21, 22, 90, 91, 40, 13a(13), and 50.

FIG. 16

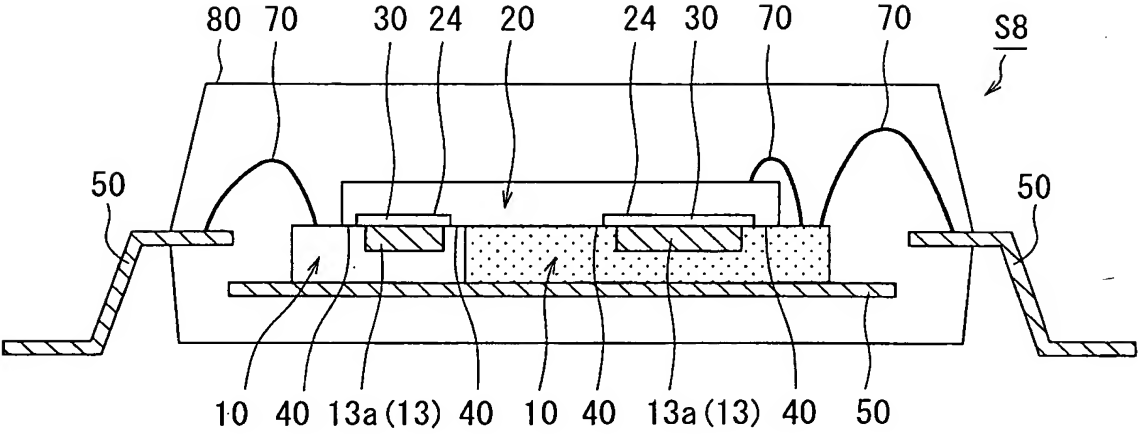


FIG. 17A

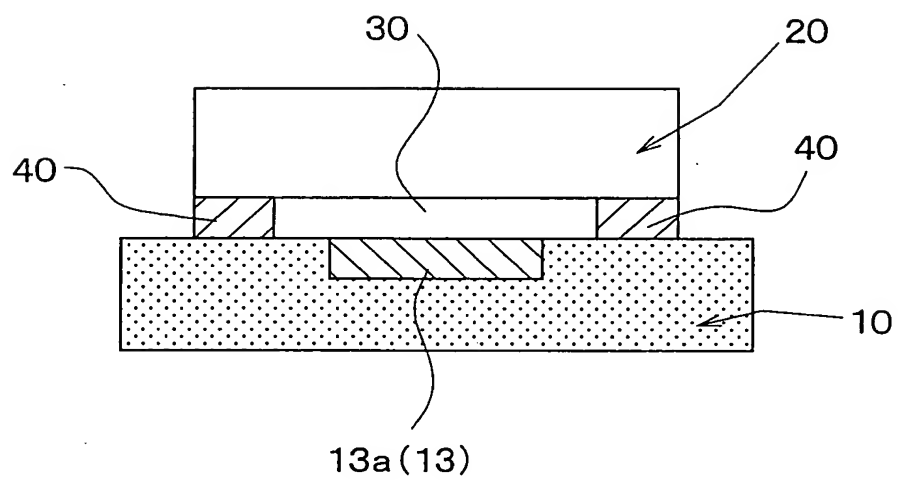


FIG. 17B

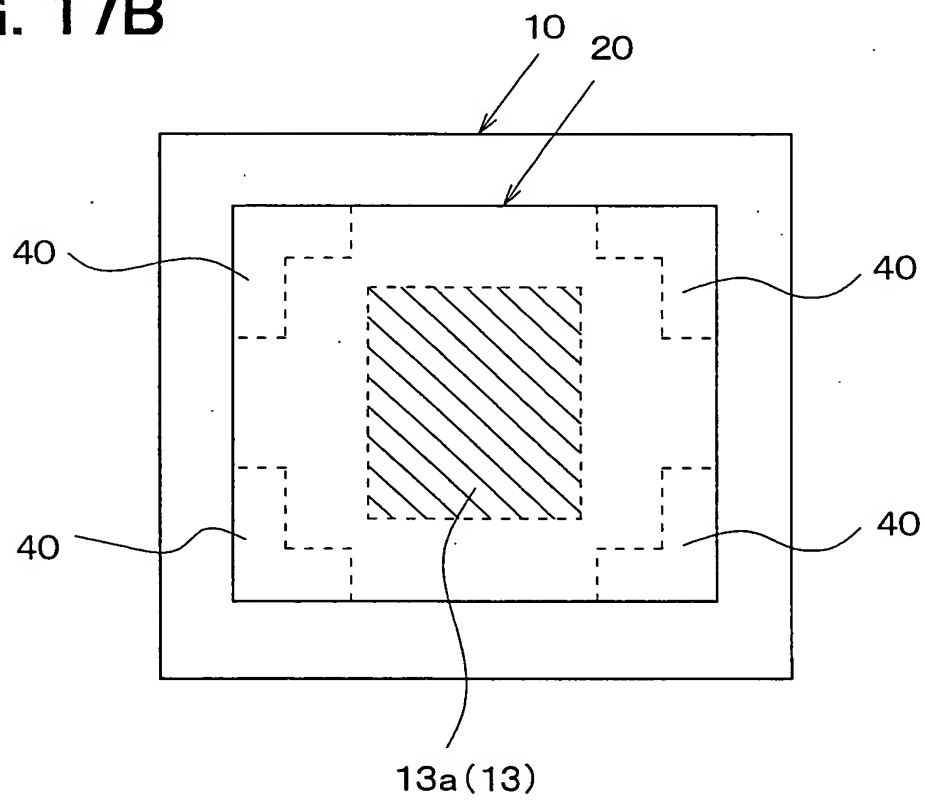


FIG. 18

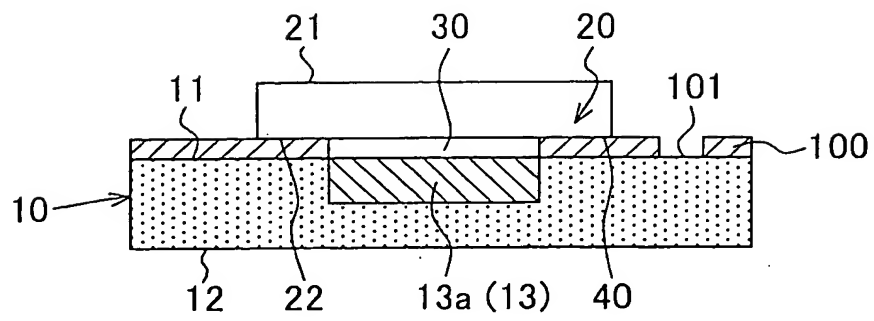


FIG. 19
RELATED ART

